This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An Integrated device in emitter switching configuration, said device being integrated in a chip of semiconductor material of a first conductivity type, said chip having a first surface and a second surface opposite to each other, said device comprising:

a first transistor having a base region, an emitter region and a collector region;

a second transistor having a not drivable terminal for collecting charges, which is connected with the emitter terminal of the first transistor; and

a quenching element that discharges current from the first transistor when said second transistor is turned off, said quenching element being coupled with the base region of the first transistor and with the not drivable terminal of the second transistor, said quenching element having at least one Zener diode made in polysilicon, said at least one polysilicon Zener diode being formed on the second surface of said chip and comprising a polysilicon layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction, wherein the emitter region of the first transistor extends as a comb having elongated portions inside the base region and the polysilicon region includes a plurality of zener diodes distributed along a perimeter of the elongated portions.

2. (Original) The Integrated device according to claim 1, wherein said chip comprises a first region of the second conductivity type which extends from the second surface into the chip and a second region of the first conductivity type which extends from the second surface into the first region, and the first region, the second region and a portion of the chip comprised between the first region and the first surface forming respectively the base region, the emitter region and the collector region of the first transistor.

3. (Original) Integrated device according to claim 2, wherein said first transistor and said second transistor are bipolar transistors and said chip comprises a third region of the second conductivity type which extends from the second surface into the second region and a fourth region of the first conductivity type which extends from the second surface into the third region, each of the second region, of the third region and of the fourth region forming respectively the collector region, the base region and the emitter region of the second transistor.

4. (Previously Presented) Integrated device according to claim 2, comprising a bipolar third transistor connected with the first transistor in a Darlington configuration wherein the emitter terminal of the first transistor is connected with a base terminal of the third transistor and the collector terminal of the first transistor is connected with a collector terminal of the third transistor.

5. (Original) Integrated device according to claim 2, wherein said second transistor is a MOS transistor and said chip comprises a couple of third regions of the second conductivity type which extend from the second surface into the second region and a couple of fourth regions of the first conductivity type which extend from the second surface into each one of third regions, each of the second region, of the third regions and of the fourth regions forming respectively the drain region, the body region and the source region of the second transistor.

6. (Original) Integrated device according to claim 1, wherein said first conductivity type of the semiconductor material is of N-type and said second conductivity type of semiconductor material is of P-type.

7. (Original) Integrated device according to claim 1, wherein said first conductivity type of the semiconductor material is of P-type and said second conductivity type of semiconductor material is of N-type.

8. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises a polysilicon Zener diode the cathode of which is

connected with the base terminal of the first transistor and the anode of which is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises only one P-N junction.

9. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises first and second polysilicon Zener diodes in back to back connection wherein the anode of the first Zener diode is connected with the anode of the second Zener diode and the cathode of the first Zener diode is connected with the base terminal of the first transistor and the cathode of the second Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises two P-N junctions.

10. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises first and second polysilicon Zener diodes in back to back connection wherein the cathode of the first Zener diode is connected with the cathode of the second Zener diode and the anode of the first Zener diode is connected with the base terminal of the first transistor and the anode of the second Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises two P-N junctions.

11. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises a series of couples of polysilicon Zener diodes in back to back connection wherein the cathode of the one Zener diode of one couple is connected with the cathode of the other Zener diode of the same couple and so on and the anode of the first Zener diode is connected with the base terminal of the first transistor and the anode of the last Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises a series of P-N junctions.

12. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode comprises a series of couples of polysilicon Zener diodes in back to back connection wherein the anode of the one Zener diode of one couple is connected with the anode of the other Zener diode of the same couple and so on and the cathode of the first Zener

diode is connected with the base terminal of the first transistor and the cathode of the last Zener diode is connected with said other not drivable terminal of the second transistor and said polysilicon layer comprises a series of P-N junctions.

13. (Original) Integrated device according to claim 1, wherein said at least one polysilicon Zener diode is formed on the second surface of the chip in a zone over an insulated layer.

14. (Original) Integrated device according to claim 1, comprising a diode the cathode of which is connected with the collector terminal of the first transistor and the anode of which is connected with said other not drivable terminal of the second transistor, said diode conducing when the voltage value at the collector terminal becomes lower than the voltage value at the other not drivable terminal of the second transistor.

15.-22. (Cancelled)

23. (Currently Amended) A device, comprising:

a semiconductor substrate of a first type of conductivity;

a first region having a second type of conductivity formed in the semiconductor substrate;

a second region having the first type of conductivity formed over and in contact with the first region, the first and second regions and a portion of the substrate underlying the first region forming base, emitter and collector, respectively, of a first transistor;

a second transistor formed in the substrate and including a third region having the first type of conductivity, formed over and in contact with the second region;

the second transistor also including a fourth region having the second type of conductivity, formed in the third region;

an insulating layer selectively formed on an upper surface of the substrate;

a polysilicon layer selectively formed on the insulating layer; and

a zener diode formed in the polysilicon layer and including first and second junction regions having first and second types of conductivity, respectively, the diode being configured to discharge current from the first region when the second transistor is turned off, wherein the second region of the first transistor extends as a comb having elongated portions inside the first region of the first transistor and the zener diode is one of a plurality of zener diodes formed in the polysilicon layer and distributed along a perimeter of the elongated portions.

24. (Original) The device of claim 23 wherein the second transistor is a bipolar transistor and further includes a fifth region having the first type of conductivity and formed in the fourth region, the third, fourth and fifth regions comprising collector, base and emitter, respectively, of the second transistor.

25. (Original) The device of claim 23 wherein the second transistor is a MOS transistor and further includes:

a fifth region having the second type of conductivity, formed in the third region and separated from the fourth region by a portion of the third region;

sixth and seventh regions having the first type of conductivity and formed in the fourth and fifth regions, respectively; and

a polysilicon region formed on the insulating layer, apart from the polysilicon layer and over the portion of the third region, the polysilicon region, the sixth and seventh regions, and the fourth region comprising gate, source and drain, respectively, of the MOS transistor.

26. (Original) The device of claim 23 wherein the zener diode is one of a plurality of zener diodes formed in the polysilicon layer, the plurality of diodes connected in series, and alternating in polarities.

27.-30. (Cancelled)

31. (Previously Presented) The integrated device of claim 1 wherein said quenching element is on a first side of the second surface, and wherein substantially all semiconducting regions are on a second side of the second surface.

32. (Previously Presented) The device of claim 23 further comprising:

the first, second, third, and fourth regions formed on a first side of the insulating layer; and

the polysilicon layer selectively formed on a second side of the insulating layer.

33. (Canceled)

34. (Currently Amended) An integrated device integrated in a chip of semiconductor material of a first conductivity type, the chip having a first surface and a second surface opposite to each other, the device comprising:

a first transistor having a control region and first and second conduction regions;

a second transistor having a control region and first and second conduction regions, the first conduction region of the second transistor being connected to the second conduction region of the first transistor; and

quenching means for discharging current from the first transistor when the second transistor is turned off, the quenching means being connected between the control terminal of the first transistor and the second conduction region of the second transistor, being positioned in a polycrystalline semiconductor layer formed on the second surface of the chip, and including a first zone of the first conductivity type and a second zone of a second conductivity type in order to form a first P-N junction, wherein the second conduction region of the first transistor extends as a comb having elongated portions inside the control region of the first transistor and the polycrystalline semiconductor layer includes a plurality of zener diodes distributed along a perimeter of the elongated portions.

35. (Previously Presented) The integrated device of claim 34, wherein the control region of the second transistor includes a first region of the second conductivity type that

extends from the second surface into the chip, the second conduction region of the second transistor includes a second region of the first conductivity type the extends from the second surface into the first region, and the first conduction region of the second transistor includes a third region of the first conductivity type positioned between the first region and the first surface.

36. (Previously Presented) The integrated device of claim 35, wherein the first transistor and the second transistor are bipolar transistors, the second conduction region of the first transistor includes the third region, the first conduction terminal of the first transistor includes a portion of the chip between the third region and the first surface, and the control region of the first transistor includes a fourth region positioned between the third region and the portion of the chip between the third region and the first surface.

37. (Previously Presented) The integrated device of claim 34 wherein the second conduction region of the first transistor includes a first buried region of the first conductivity type, the control region of the first transistor includes a second buried region of the second conductivity type, and the first conduction region includes a portion of the chip between the second buried region and the first surface.

38. (Previously Presented) The integrated device of claim 37 wherein the second conduction region of the second transistor includes a region of the first conductivity type extending from the second surface into the chip, the device further comprising:

a sinker region that extends from the second surface of the chip to the second buried region;

a first conductive connector positioned on the second surface and connecting the sinker region to the first zone; and

a second conductive connector positioned on the second surface and connecting the second conduction region of the second transistor to the second zone.

39. (Previously Presented) The integrated device of claim 34 wherein the first transistor is a bipolar transistor and the second transistor is a field-effect transistor.

40. (Previously Presented) The integrated device of claim 34, further comprising a bipolar third transistor connected with the first transistor in a Darlington configuration wherein an emitter terminal of the first transistor is connected with a base terminal of the third transistor and a collector terminal of the first transistor is connected with a collector terminal of the third transistor.

41. (Previously Presented) The integrated device of claim 40 wherein the quenching means includes first and second zener diodes connected respectively between the second conduction terminal of the second transistor and base terminals of the first and third transistors.

42. (Previously Presented) The integrated device of claim 34 wherein the quenching means includes first and second zener diodes in back to back connection.

43. (Previously Presented) The integrated device of claim 34, further comprising an insulating layer positioned between the polycrystalline semiconductor layer and the second surface of the chip.

44. (Canceled)